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- (57) A compensated pixel driver circuit for an organic electroluminescent device, wherein the circuit comprises a unity gain buffer which is preferably implemented as an operational amplifier. The circuit provides a unity gain sample and hold function, thereby compensating the current supply to the electroluminescent element by providing a self adjusting load.

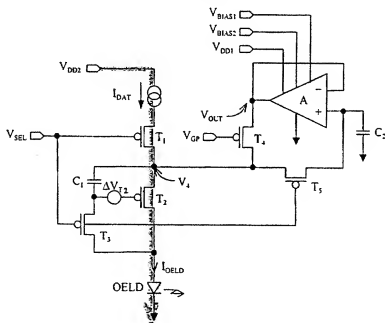


Figure 3

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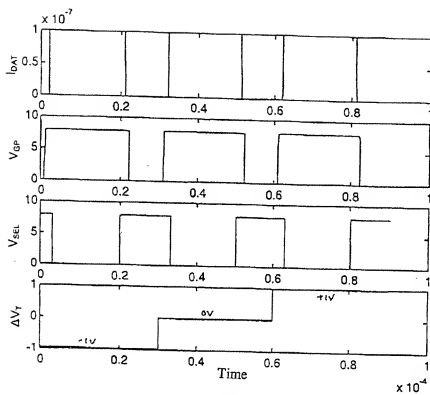


Figure 2B

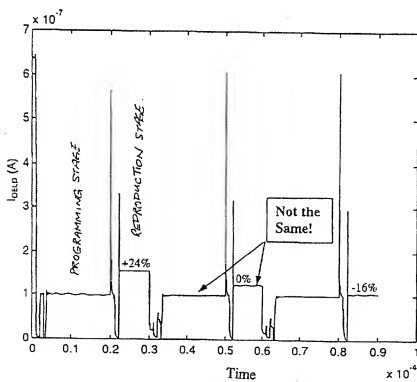


Figure 2C



Open-Loop Gain (OLG)	>20
$V_{DD}$	9 V
$V_{SS}$	0 V
$V_{OUT}$	1 V – 8 V
Inverting Input ( $V_-$ )	$= V_{OUT}$
Non-Inverting Input ( $V_+$ )	1 V – 8 V
Max Output Current	1 $\mu$ A
Settle Time	<20 $\mu$ s
Offset Voltage	Minimal
Quiescent Current	Minimal
Space Occupation	< 210 $\times$ 70 $\mu$ m <sup>2</sup>

Single Power Supply  
Rail to Rail

Figure 4

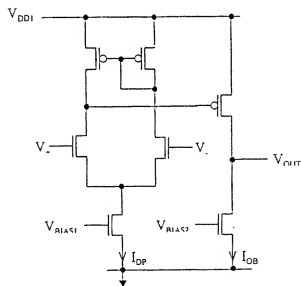


Figure 5

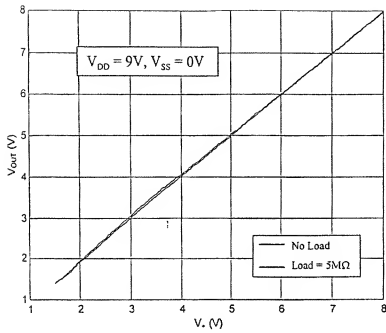


Figure 6

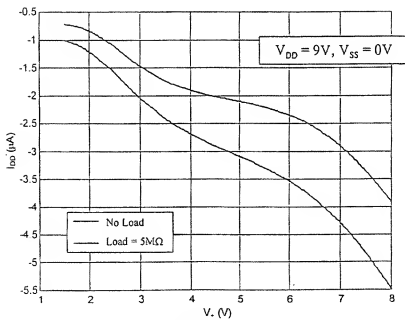


Figure 7

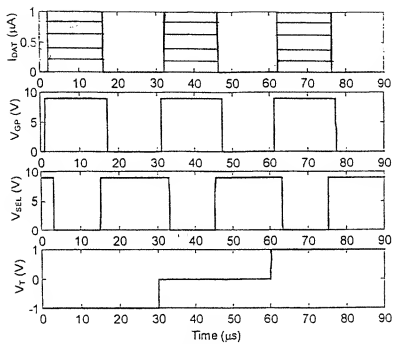


Figure 8

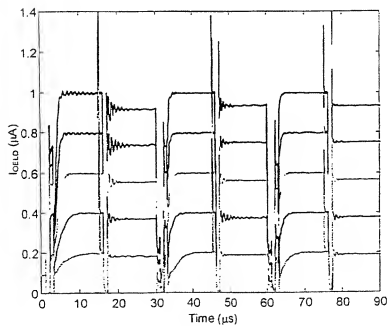


Figure 9

## Organic ElectroLuminescent Device

## Compensated Pixel Driver Circuit

The present invention relates to an organic electroluminescent device and particularly to a compensated pixel driver circuit thereof.

An organic electro-luminescent device (OLED) consists of a light emitting polymer (LEP) layer sandwiched between an anode layer and a cathode layer. Electrically, this device operates like a diode. Optically, it emits light when forward biased and the intensity of the emission increases with the forward bias current. It is possible to construct a display panel with a matrix of OLEDs fabricated on a transparent substrate and with one of the electrode layers being transparent. One can also integrate the driving circuit on the same panel by using low temperature polysilicon thin film transistor (TFT) technology.

In a basic analog driving scheme for an active matrix OLED display, a minimum of two transistors are required per pixel (Figure 1):  $T_1$  is for addressing the pixel and  $T_2$  is for converting the data voltage signal into current which drives the OLED at a designated brightness. The data signal is stored by the storage capacitor  $C_{\text{storage}}$  when the pixel is not addressed. Although p-channel TFTs are shown in the figures, the same principle can also be applied for a circuit with n-channel TFTs.

There are problems associated with TFT analog circuits and OLEDs do not act like perfect diodes. The LEP material does, however, have relatively uniform characteristics. Due to the nature of the TFT fabrication technique, spatial variation of the TFT characteristics exists over the entire panel. One of the most important considerations in a TFT analog circuit is the variation of threshold voltage,  $\Delta V_T$ , from device to device. The effect of such variation in an OLED display, exacerbated by the non perfect diode behaviour, is the non-uniform pixel



brightness over the display panel, which seriously affects the image quality. Therefore, a built-in compensation circuit is required.

A simple threshold voltage variation compensation, current driven, circuit has been proposed. The current driven circuit, also known as the current programmed threshold voltage compensation circuit is illustrated in figure 2A. In this circuit,  $T_1$  is for addressing the pixel.  $T_2$  operates as an analog current control to provide the driving current.  $T_3$  connects between the drain and gate of  $T_2$  and toggles  $T_2$  to be either a diode or in saturation.  $T_4$  acts as a switch. Either  $T_1$  or  $T_4$  can be ON at any one time. Initially,  $T_1$  and  $T_3$  are OFF, and  $T_4$  is ON. When  $T_4$  is OFF,  $T_1$  and  $T_3$  are ON, and a current of known value is allowed to flow into the OELD, through  $T_2$ . This is the programming stage because the threshold voltage of  $T_2$  is measured with  $T_2$  operating as a diode (with  $T_3$  turned ON) while the programming current is allowed to flow through  $T_1$ , through  $T_2$  and into the OELD.  $T_3$  shorts the drain and gate of  $T_2$  and turns  $T_2$  in to a diode. The detected threshold voltage of  $T_2$  is stored by the capacitor  $C_1$  connected between the gate and source terminals of  $T_2$  when  $T_3$  and  $T_1$  are switched OFF. Then  $T_4$  is turned ON, the current is now provided by  $V_{DD}$ . If the slope of the output characteristics were flat, the reproduced current would be the same as the programmed current for any threshold voltage of  $T_2$  detected. By turning ON  $T_4$ , the drain-source voltage of  $T_2$  is pulled up, so a flat output characteristic will keep the reproduced current the same as the programmed current. Note that  $\Delta V_{T2}$  shown in figure 2A is imaginary, not real.

A constant current is provided, in theory, during the active programming stage, which is  $t_3$  to  $t_4$  in the timing diagram shown in figure 2A. The reproduction stage starts at  $t_6$  and ends at  $t_1$  of the next cycle.

In practice, there is always a slope in the output characteristics, so the reproduced current is not the same as the programmed current. This issue limits the device channel length of the polysilicon TFTs because of the increase of the short channel effect in polysilicon TFTs when the device channel length gets smaller. Simulations show that the variation between the reproduced current and programmed current is unacceptable for  $L = 4\mu\text{m}$  and below. This limitation on the design of transistor  $T_2$  is a very serious practical problem, especially when small data currents are used. It is therefore important to find a technique that will provide good compensation in short channel devices.

The driving waveforms used are shown in timing chart fashion in figure 2B. The threshold voltage  $V_T$  shown at the bottom of figure 2B is that for transistor  $T_2$ . As can be seen from figure 2B, this threshold voltage has a range of  $-1\text{V}$  to  $+1\text{V}$ . Such a range is much larger than the variation  $\Delta V_T$  across a practical OLED matrix.

Typical variation between the reproduced current and programmed current supplied to the OLED is illustrated in figure 2C. Figure 2C illustrates three cycles of OLED current supply: one from 0 to  $30\mu\text{s}$ , one from  $30\mu\text{s}$  to  $60\mu\text{s}$ , and one from  $60\mu\text{s}$  to  $90\mu\text{s}$ . The first half of each of these cycles is the programming stage and the second half of the cycle is the reproduction stage. It is to be noted that the current output levels in the reproduction stage compared with those in the corresponding program stage are remarkably different from each other.

According to a first aspect of the present invention there is provided a compensated pixel driver circuit for an organic electroluminescent device, wherein the circuit comprises a unity gain buffer. Preferably the unity gain buffer is implemented as an operational amplifier.

According to a second aspect of the present invention there is provided a method of compensating the current supply to an organic electroluminescent pixel comprising the step of using a unity gain buffer to provide a self adjusting load.

According to a third aspect of the present invention there is provided an organic electroluminescent display device comprising one or more compensated pixel driver circuits according to the first aspect of the invention.

Embodiments of the present invention will now be described by way of example only and with reference to the accompanying drawings, in which:-

Figure 1 shows a conventional OLED pixel driver circuit using two transistors,

Figure 2 shows a current programmed OLED driver with threshold voltage compensation,

Figure 3 shows a compensated pixel driver circuit according to an embodiment of the present invention,

Figure 4 is a table of requirements for one specific example of an operational amplifier which can be used in the circuit of figure 3,

Figure 5 is an example of a circuit for implementing the operational amplifier shown in figure 3,

Figure 6 is a graph illustrating the unity-gain buffer characteristics of the compensating circuit of figure 3,

Figure 7 is a graph illustrating the total required supply current,

Figure 8 is a driving waveform timing diagram, and

Figure 9 illustrates the current output to the OLED using the circuit of figure 3.

A compensated pixel driver circuit according to an embodiment of the present invention is shown in figure 3. Compared with the circuit of figure 2, there is added an operational amplifier OpAmp A, a capacitor  $C_2$  and a transistor  $T_5$ . As shown in figure 3,  $V_{out}$  of the OpAmp is connected to the inverting input  $V_-$  thereof. The OpAmp thus has unity gain. Capacitor  $C_2$  ensures a sample and hold function and transistor  $T_5$  acts as a control switch to store the voltage on  $C_2$ . In effect the circuit provides a self-adjusted load or voltage source ( $V_{DD}$ ) and by thus

holding the operative voltage constant the effect of the slope in the output characteristics can be avoided. In its generic form, the OpAmp A is a unity gain buffer having its input connected to the source-drain path of transistor  $T_5$  and its output connected to the source-drain path of transistor  $T_4$ , the input being connected to ground via capacitor  $C_2$ .

As shown in figure 3, a TFT operational amplifier configured as a sample and hold circuit is used to provide a variable  $V_{DD}$  so that the drain-source voltage of  $T_2$  in the reproduction stage is the same as that during the programming stage. During the programming stage, the voltage at the source of  $T_2$  is passed to the storage capacitor  $C_2$  at the input of the unity-gain OpAmp. The output of the OpAmp faithfully reproduces the voltage and also provides the current to the OELD through  $T_2$ . The driving waveform is the same as that for the circuit of figure 2.

The program current path is from  $V_{DD2}$  through node  $V_4$ ,  $T_1$ ,  $T_2$  and the OELD. The reproduction current path is from  $V_{DD1}$ , through the OpAmp,  $V_{out}$ ,  $T_4$ , node  $V_4$ ,  $T_2$  and the OELD.

In the circuit of figure 3, the voltage at point  $V_4$  is substantially the same in the reproduction cycle to the voltage at that point in the programming cycle. Additionally, a very high Open-Loop Gain (OLG) is not required in contrast to usual TFT circuits. An advantage of the embodiment of the present invention shown in figure 3 is that the current flow to the OELD during the reproduction cycle is less sensitive to the variation in the output  $V_{out}$  of the OpAmp than  $\Delta V_{T2}$  detection of the same percentage error. Furthermore, the OpAmp design constraints are not stringent.

Figure 5 is a circuit diagram of one arrangement for implementing the OpAmp shown in figure 3. The specific requirements for this circuit are shown in the table of figure 4. Of particular note is the minimal off-set voltage. Typically this might be a few millivolts, in contrast

to the variation of several volts which may typically arise in the conventional arrangement due to the slope of the output characteristics. The circuit of figure 5 essentially consists of a differential pair circuit and a driver. The differential pair circuit comprises the top two transistors connected to the  $V_{DD1}$  rail, the respective transistors having their gates providing the two input terminals of the OpAmp, and the transistor whose gate receives  $V_{bias1}$ . The output driver comprises a transistor receiving  $V_{bias2}$  at its gate and a transistor connected between the  $V_{DD1}$  rail and  $V_{out}$ .

All of the transistors of the circuit of figure 5 are TFTs having a channel length of  $10\mu\text{m}$  (in contrast to  $T_2$ ). This channel length avoids the devices being stressed by the high value of  $V_{DD}$ . The transistor connected between the  $V_{DD1}$  rail and  $V_{out}$  has a channel width of  $100\mu\text{m}$  in order to ensure sufficient current output. The area required to implement the circuit of figure 5 can be reduced by varying the W/L absolute size ratio of the transistors, subject to a corresponding reduction in the maximum drive current. The space occupation value of  $270\mu\text{m} \times 70\mu\text{m}$  given in the table of figure 4 can, for example, be reduced to approximately  $130\mu\text{m} \times 10\mu\text{m}$ , subject to a reduction in the maximum drive current from  $5\mu\text{A}$  to  $1.5\mu\text{A}$ . However, in practice a maximum drive current of  $1\mu\text{A}$  might suffice (as indicated in figure 4).

In the specific example given, the current  $I_{DP}$  flowing through the differential pair circuit has a maximum value of  $1\mu\text{A}$  and the current  $I_{OB}$  flowing through the driver circuit has a maximum value of  $5\mu\text{A}$ . The additional current required by the presence of the OpAmp is thus minimal.

Figure 6 is a graph illustrating the unity-gain buffer characteristics of the compensating circuit of figure 3. As shown, the plot of  $V_{out}$  against  $V_+$  is the same for both the load and the

no-load conditions. The load condition is  $5M\Omega$ , which corresponds to a current of  $1\mu A$  through the OELD.

The total current supply required by the OpAmp of figure 3, in one specific example, is shown in figure 7. The total current supply required is that required by the differential pair circuit (figure 5), that required by the OpAmp driver circuit (figure 5) and that required to drive the OELD. Again load ( $5M\Omega$ ) and no-load conditions are shown.

The driving waveforms used with one implementation of the circuit of figure 3 are shown in timing chart fashion in figure 8. Of course, the threshold voltage  $V_T$  shown at the bottom of figure 8 is that for transistor  $T_2$ . As can be seen from figure 8, this threshold voltage has a range of  $-1V$  to  $+1V$ . Such a range is much larger than the variation  $\Delta V_T$  across a practical OELD matrix. Threshold variation  $\Delta V_T$  in other transistors ( $T_1, T_3, T_4, T_5$ ) have little effect as they are used as switches and operate under voltage ranges greater than  $\Delta V_T$ .

The output current supplied to the OELD using the circuit of figure 3 is illustrated in figure 9. Figure 9 illustrates three cycles of OELD current supply: one from 0 to  $30\mu s$ , one from  $30\mu s$  to  $60\mu s$ , and one from  $60\mu s$  to  $90\mu s$ . The first half of each of these cycles is, of course, the programming stage and the second half of the cycle is the reproduction stage. In each cycle, five different program currents are illustrated (ie vertically – at 0.2, 0.4, 0.6, 0.8 and 1.0). It is to be noted that the current output levels in the reproduction stage compared with those in the corresponding program stage are remarkably close. The comparison is slightly less good for larger program currents, but is still relatively small. Moreover, the difference can be predicted (as shown in figure 9) and can therefore be included in a gamma compensation (eg use  $1.1\mu A$  instead of  $1\mu A$  in the programming stage).

It will be apparent to persons skilled in the art that variations and modifications can be made to the arrangements described with respect to figure 3 to 9 without departing from the scope of the invention.

## CLAIMS

1. A compensated pixel driver circuit for an organic electroluminescent device, wherein the circuit comprises a unity gain buffer.
2. A compensated pixel driver circuit as claimed in claim 1, wherein the unity gain buffer is implemented as an operational amplifier.
3. A compensated pixel driver circuit as claimed in claim 1 or claim 2, wherein the buffer is connected to have unity gain.
4. A compensated pixel driver circuit as claimed in claim 2, wherein the circuit comprises a transistor connected so as to act as a current switch for storing voltage on the said capacitor.
5. A compensated pixel driver circuit as claimed in any preceding claim, wherein the buffer comprises a differential pair circuit and a driver circuit.
6. A compensated pixel driver circuit as claimed in claim 5, wherein the differential pair circuit comprises two transistors whose gates respectively provide an inverting input and a non-inverting input of the buffer and a further transistor whose gate provides a bias voltage input of the buffer.



7. A compensated pixel driver circuit as claimed in claim 5 or claim 6, wherein the driver circuit comprises two transistors connected in series with the output of the buffer being taken from the said connection between these transistors.

8. A compensated pixel driver circuit as claimed in any preceding claim, wherein the circuit is implemented with polysilicon thin film transistors.

9. A method of compensating the current supply to an organic electroluminescent pixel comprising the step of using an buffer to provide a self adjusting load.

10. An organic electroluminescent display device comprising one or more compensated pixel driver circuits as claimed in any of claims 1 to 8.



Application No: GB 0007879.0  
Claims searched: All

11

Examiner: Rowland Hunt  
Date of search: 30 May 2000

## Patents Act 1977 Search Report under Section 17

### Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): G5C (CHBN)

Int Cl (Ed.7): G09G 3/32

Other: Online: EPODOC, JAPIO, WPI

### Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	GB 2337354 A (FUTABA DENSHI KOGYO)	
A	EP 0365445 A2 (EASTMAN KODAK)	
A	US 5714968 (IKEDA)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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